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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,725	01/30/2001	Mitsuaki Osame	SEL 237	1317

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EXAMINER	
OSORIO, RICARDO	
ART UNIT	**PAPER NUMBER**
2673	9

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/772,725	OSAME ET AL.	
	Examiner	Art Unit	
	RICARDO L OSORIO	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,17,18 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 17,18 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 21-26 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: New claims 21, 23 and 25 are directed to a dummy gate signal line, which constitutes a third subcombination.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 21-26 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

1. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwon (6,124,840).

Regarding claims 17 and 19, Kwon teaches of a semiconductor display device comprising a TFT source signal line drive circuit unit (Fig. 3, reference character 20) and a TFT gate signal line drive circuit unit (Fig. 3, reference character 30) formed over a substrate, said gate signal line drive circuit having at least one tristate buffer per gate signal line and gate selection pulse change-over switches (Fig. 12, and col. 7, lines 18-23); said tristate buffer comprising: at least a first circuit and a second circuit (see Fig. 12. first top two transistors are first circuit and second bottom two transistors are second circuit); a first power source electrically connected to said first circuit (Fig. 12, VDD); a second power source having a potential lower than that of said first power source (IN, it is inherent that a second power source with a potential lower than VDD is needed to provide signal IN); and a third power source having a potential lower than that of said second power source and electrically connected to said second circuit (VSS, it is inherent that ground, or low potential VSS has to be lower than the potential used at central point of the two circuits to provide IN).

Regarding claims 18-20, Kwon teaches than the semiconductor display device is incorporated in a television (col. 1, lines 39-42).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Kobayashi et al (5,936,455).

Regarding claim 1, Kwon further teaches of a pixel unit in which plural TFTs are arranged like a matrix (col. 2, lines 41-46).

However, Kwon fails to teach of the tristate buffer comprising of a first circuit including a pair of n-channel and p-channel TFTs; a second circuit including a pair of n-channel and p-channel TFTs, the source region of the n-channel TFT in the first circuit is electrically connected, at a first connection point, to the source region of the p-channel TFT of the second circuit; a first power source is electrically connected to the source region of the p-channel TFT of the first circuit; a second power source having a potential lower than that of the first power source is electrically connected to the first connection point; a third power source having a potential lower than the second power source is electrically connected to the source region of the n-channel TFT of the second circuit; and an output signal line of the first circuit and an output signal line of the second circuit are both electrically connected to the gate line at a second connection point.

Kobayashi teaches of a tristate buffer (see Fig. 3) having a first circuit including a pair of n-channel and p-channel TFTs (Fig. 3, reference characters 21 and 22); a second circuit including a pair of n-channel and p-channel TFTs (Fig. 3, reference characters 23 and 24), the source region of the n-channel TFT in the first circuit is electrically connected, at a first connection point, to the source region of the p-channel TFT of the second circuit (Fig. 23, connection between transistors 22 and 23); a first power source is electrically connected to the source region of the p-channel TFT of the first circuit (Fig. 3, Vcc); a second power source having a potential lower

than that of the first power source is electrically connected to the first connection point (Fig. 3, reference character 27); a third power source having a potential lower than the second power source is electrically connected to the source region of the n-channel TFT of the second circuit (Fig. 3, Gnd); and an output signal line of the first circuit and an output signal line of the second circuit are both electrically connected to the gate line at a second connection point.(Fig. 23, reference character DO(2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the tristate buffer, as taught by Kobayashi, in the device of Kwon to provide a MOS-IC requiring low power consumption by efficiently reusing electrical charges discharged from the gate (col. 1, lines 47-49).

Response to Arguments

2. Applicant's arguments filed December 15, 2003 have been fully considered but they are not persuasive.

Applicant argues that Kwon does not disclose or suggest that the gate signal line drive circuit has at least one tristate buffer and one gate selection pulse change-over switch.

Examiner disagrees because Kwon teaches of at least one tristate buffer per gate signal line and gate selection pulse change-over switches (Fig. 12, and col. 7, lines 18-23);

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ricardo L. Osorio whose telephone number is (703) 305-2248. The examiner can normally be reached on Mon-Thu from 7:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached at 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Ricardo L. Osorio
Examiner
Art Unit: 2673

RLO
March 7, 2004